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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,553	06/20/2001	Lars-Peter Heineck	GR 98 P 1379 D	6319

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,553	HEINECK ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 and 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statements of papers No. 4 and 5 (three pages with lists).

Specification

The examiner objects to the disclosure. In particular, the text of the disclosure on page 11, in which it is stated that "This produces a "bird's beak" 5 or a thickened area of the gate oxide 2 in the region below the side wall 22 of the gate 3" is contradicted by Figure 2, in which no such thickened area is visible, as well as by Figure 3, in which there is no such thickened area below the gate oxide 2: instead, in Figure 3 the bird's beak 5 is located below the gate 3 itself. The resulting discrepancy should be removed, either by changing the wording on page 11 of the disclosure or by producing amended Figures 2 and 3.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1 and 5-6*** are rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al. (5,612,249).

With regard to claim 1: Sun et al teach (cf. Figure 20) a MOS transistor that may be used as a single-transistor memory cell, comprising: a semiconductor substrate 1 that may be either p- or n-type semiconductor material (cf. column 4, lines 50-52), hence a semiconductor substrate having a substrate surface, a first conductive region and second conductive region (source and drain regions 24 (cf. column 8, lines 48-52); a gate oxide 5/14 (cf. column 5, lines 24-33 and column 7, lines 12-27; note that the material constitution of regions 5 and 14 are prescribed in identical manner: both regions are to be made by oxidation of silicon; hence from the device point of view the regions 5 and 14 constitute a contiguous entity) disposed on said substrate surface; a gate 6/18 (cf. column 5, lines 34-37 and column 7, lines 65-67: note that regions 6 and 18 both materially are defined in exactly the same manner: they should consist of either poly or amorphous silicon; the distinction between gate 6 and interconnect 18 is thus from a device point of view moot, as both regions are materially identically specified and are, as gate and gate interconnect, required to have the same electrically conductive requirements) disposed on said gate oxide over an area between said first and second conductive regions (cf. Figure 20); and an insulating spacer 23 (cf. column 8, lines 40-43) disposed on said side wall of said gate, said spacer acting inherently as oxidation barrier (because material can burn only once); said gate oxide insulating said gate (note that the material constitution of the gate oxide is prescribed as the product of the oxidation of silicon, hence silicon oxide; see column 5, line 27; and column 7, lines 12-

15) and having a thickened area below said side wall 23 of said gate. In conclusion, Sun et al anticipate claim 1.

With regard to claim 5: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67).

With regard to claim 6: said gate taught by Sun et al is specifically allowed to include a tungsten silicide layer (column 8, lines 13-18 and Figure 17) and a polysilicon layer (cf. column 5, lines 34-37 and column 7, lines 65-67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 2-3 and 4*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al (5,612,249) in view of Ahmad (6,037,639). As detailed above, Sun et al anticipate claim 1.

With regard to claim 2: In the specific embodiment of Figure 20 discussed in connexion with claim 1, Sun et al do not necessarily specify the insulating spacer to be a silicon nitride spacer. However, Sun et al do make use of nitride spacers in the embodiment illustrated by Figure 12 and discussed in column 6, lines 49-64. Furthermore, the use of nitride side wall spacers in the art of MOS transistors for the

purpose of improving hot carrier resistance in ULSI transistors (cf. abstract, column 1, lines 6-10, and column 2, lines 12-16). The motivation to combine Ahmad's teaching of nitride side wall spacers with the invention of Sun et al is to improve hot carrier resistance for reduced transistor size (with a reduction of transistor size the electric field increases and hence improved protection is needed). The invention can be easily combined by a simple replacement of the oxide spacers by nitride spacers. Reasonable expectation of success is justified because of the long-standing experience in the application of nitrogen implantation.

With regard to claim 3: said gate taught by Sun et al is specifically allowed to be include a layer of polysilicon (cf. column 5, lines 34-37 and column 7, lines 65-67).

With regard to claim 4: Sun et al teach a layer of tungsten-silicide film 20 deposited on the polysilicon gate layer 18 (see Figure 17 and column 8, lines 13-18). Therefore, the primary reference teaches the further limitations defined by claim 4.

5. ***Claims 7-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al (5,612,249) in view of Krautschneider (5,854,500). As detailed above, Sun et al anticipate claim 1 (on which claim 8 depends). Sun et al do not necessarily teach the further limitation of claim 8. As shown by Krautschneider (front figure), however, lateral MOS transistors with attributes as taught by Sun et al, particularly with gate oxide 110 (see in Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20) for instance have long been applied as selection transistors to DRAM

memory cells (cf. abstract, first sentence). The further limitation of claim 8 thus only represents an obvious use of said MOS transistors.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Soshiro (JP405129595A).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
May 23, 2002